Please amend the claims as follows (this listing replaces all prior versions):

1. (currently amended) An active matrix display device comprising an array of pixels a set of row conductors through which rows of pixels are selected, a set of column conductors through which data signals are supplied to selected pixels, each pixel comprising a plurality of sub pixels in which sub pixels are each associated with a respective switching transistor for controlling the supply of a data signal to the sub pixel,

wherein the plurality of sub pixels of a pixel are coupled to a column conductor associated with the pixel via a common switching transistor through which data signals are supplied to the sub pixels, and

wherein the device is selectively operable in a first mode in which the plurality of sub-pixels of a pixel are addressed simultaneously with a data signal and in a second mode in which the sub pixels of a pixel are addressed individually with respective data signals.

2. (previously presented) The display device according to claim 1, wherein the device comprises drive means for providing data signals to the column conductors and switching signals to the row conductors, and wherein the drive means is operable in the first mode to switch the switching transistors associated with the sub pixels of a pixel at the same time so as to supply a data signal on the associated column conductor to each sub pixel, and wherein the drive means is operable in the second mode to switch the switching transistors associated with the sub pixels of the pixel selectively in sequence such that data signals on the associated column conductor are supplied to respective sub pixels.

3. (previously presented) The display device according to claim 1, wherein the sub pixels of a pixel are connected in serial manner with the input terminal of the switching transistor associated with the first sub pixel of the series being connected to the associated column address conductor and with the input terminal of the switching transistor associated with each of the

other sub pixels in the series being connected to the output terminal of the switching transistor associated with the preceding sub pixel in the series.

4. (previously presented) The display device according to claim 1, wherein the sub pixels of a pixel are connected in parallel manner with the input terminal of the switching transistor associated with one sub pixel being connected to the associated column address conductor and with the input terminals of the switching transistors associated with the other sub pixels being connected to the output terminal of the switching transistor associated with the one pixel.

5. (previously presented) The display device according to claim 1, wherein the control electrodes of the switching transistors associated with the sub pixels of a pixel are connected to respective different row conductors.

6. (previously presented) The display device according to claim 1, wherein each pixel comprises first and second sub pixels, wherein the control electrodes of the switching transistors associated with the first and second sub pixels of a pixel are connected to first and second row conductors respectively,

wherein, for each pixel, the input of the switching transistor associated with the first sub pixel is connected to the associated column conductor and the input of the switching transistor associated with the second sub pixel is connected to the output of the switching transistor associated with the first sub pixel,

wherein the first row conductor connected to one pixel is connected also to the control electrode of the switching transistor associated with the second sub pixel of another pixel connected to the associated column conductor, and

wherein the second row conductor connected to the one pixel is connected also to the control electrode of the switching transistor associated with the first sub pixel of a further pixel connected to the associated column address conductor.

7. (previously presented) The display device according to claim 1, wherein the sub pixels comprise liquid crystal picture elements connected to the outputs of their associated switching transistor.

8. (previously presented) The display device according to claim 7, wherein at least two sub pixels of a pixel are of different areas.

9. (previously presented) The display device according to claim 1, wherein the common switching transistor corresponds to the respective switching transistor of one of the plurality of sub pixels.

10. (currently amended) The display device according to claim 1, wherein each of the common switching transistor and the respective switching transistors comprise an input terminal, an output terminal and a gate terminal, wherein the [[gate]] input terminal of the common switching transistor is connected to the column conductor associated with the pixel and the output terminal of the common switching transistor is connected to at least one of the input terminals of the respective switching transistors.

11. (previously presented) The display device according to claim 10, wherein the output terminal of the common switching transistor is connected to each of the input terminals of the respective switching transistors.

12. (previously presented) The display device according to claim 10, wherein the output terminal of a first one of the respective switching transistors is connected to the input terminal of a second one of the respective switching transistors.

13. (new) The display device of claim 1, further comprising a timing and control unit for controlling a row drive circuit and a column drive circuit that provide driving signals and the

data signals to the array of pixels, the timing and control unit selectively switching between the first mode of operation and the second mode of operation in response to a mode selection control signal.

14. (new) The display device of claim 1, further comprising a timing and control unit, a row drive circuit, and a column drive circuit that are operable in the first mode to switch the switching transistors associated with the sub pixels of a pixel at the same time so as to supply a data signal on the associated column conductor to each sub pixel, and wherein the timing and control unit, row drive circuit, and column drive circuit are operable in the second mode to switch the switching transistors associated with the sub pixels of the pixel selectively in sequence such that data signals on the associated column conductor are supplied to respective sub pixels.

15. (new) The display device of claim 1 in which each sub pixel corresponds to a switching transistor and the switching transistor or transistors of a pixel other than the common switching transistor are turned on during the first mode of operation for a period of time longer than that during the second mode of operation.

16. (new) The display device of claim 1, further comprising at least one digital-to-analog converter that provides a data signal to the plurality of sub-pixels of the pixel when the display device is operating in the first mode, and the at least one digital-to-analog converter is turned off when the display device is operating in the second mode.

17. (new) The display device of claim 1 in which when the display device is operating in the first mode, the plurality of sub-pixels of a pixel are addressed simultaneously with a data signal having a level selectable from a first number of levels, and when the display device is operating in the second mode, the sub pixels of a pixel are addressed individually with respective data signals each having a level selectable from a second number of levels, the second number being smaller than the first number.

18. (new) The display device of claim 17 in which the second number is equal to 2.

19. (new) An active matrix device comprising:

a plurality of pixels, each pixel having at least two sub pixels;

a plurality of column conductors and a plurality of row conductors for addressing the pixels;

a first row conductor that controls a signal path between one of the pixels and one of the column conductors, the first row conductor controlling a signal path between two sub pixels of another pixel; and

a second row conductor that controls a signal path between the other pixel and one of the column conductors.

20. (new) The active matrix device of claim 19, wherein the sub pixels of each pixel are ratioed.

21. (new) The active matrix device of claim 20, wherein each pixel consists of two ratioed sub pixels.

22. (new) An apparatus comprising:

an array of pixels in which each pixel comprises at least one pair of sub pixels;

column conductors each being connected to the pixels of one column of the array of pixels; and

row conductors in which two or more of the row conductors are connected to the pixels of one row of the array of pixels;

wherein each of the pairs of sub pixels is associated with a circuit for connecting to a column conductor and two row conductors, the circuit comprising:

a first switching transistor with its input terminal connected to the column conductor, its output connected to the first sub pixel in the pair, and its control terminal connected to the first row conductor; and

a second switching transistor associated with its input terminal connected to the output terminal of the first switching transistor, its output terminal connected to the second sub pixel in the pair, and its control terminal connected to the second row conductor.

23. (new) The apparatus of claim 22, further comprising a display controller for providing data signals to the column conductors and switching signals to the row conductors,

the display controller being selectively operable in a first mode to switch the switching transistors associated with the sub pixels of a pixel at the same time so as to supply a data signal on the associated column conductor to each sub pixel, and

the display controller being selectively operable in a second mode to switch the switching transistors associated with the sub pixels of the pixel selectively in sequence such that data signals on the associated column conductor are supplied to respective sub pixels.

24. (new) The apparatus of claim 23, wherein at least two sub pixels of a pixel are of different areas.

25. (new) The apparatus of claim 24, wherein the ratios of the areas of the sub pixels in a pixel are powers of two.

26. (new) The apparatus of claim 22, wherein at least some row conductors are connected to two pixels in the same column.

27. (new) A method comprising:

driving a display device in a first mode in which a plurality of sub-pixels of each of an array of pixels of the display device are addressed simultaneously with a data signal; and

driving a display device in a second mode in which the sub pixels of each pixel are addressed individually with respective data signals;

wherein the display device comprises a set of row conductors through which rows of pixels are selected, a set of column conductors through which data signals are supplied to selected pixels, and each sub pixel is associated with a respective switching transistor for controlling the supply of the data signal to the sub pixel.

28. (new) The method of claim 27, further comprising selectively switching between the first mode and the second mode in response to a mode selection control signal.

29. (new) The method of claim 27 in which driving the display device in the first mode comprises:

driving the voltage on all row conductors connected to gate terminals of switching transistors associated with each sub pixel of a target pixel to a voltage level representing the logical on state;

driving the voltage on a column conductor connected to the target pixel to a level representing a data signal; and

after the sub pixels of the target pixel have been charged to a voltage corresponding to the voltage on the column conductor, driving the voltage on the row conductor connected to the gate terminal of a select transistor of the target pixel to a voltage level representing the logical off state, wherein the select transistor is the only transistor in the pixel circuit that is directly connected to the column conductor.

30. (new) The method of claim 29, wherein the data signal represents a grayscale value of a pixel in an image.

31. (new) The method of claim 29, wherein the data signal represents a grayscale value of one color component of a pixel in an image.

32. (new) The method of claim 29 in which driving the display device in the first mode comprises maintaining the voltage on the row conductor connected to the gate terminal or terminals of switching transistors other than the select transistor of the target pixel at a level representing the logical on state after the voltage on the row conductor connected to the gate terminal of the select transistor of the target pixel is driven to a level representing the logical off state.

33. (new) The method of claim 27 in which driving the display device in the second mode comprises:

driving the voltage on a row conductor connected to a gate terminal of a select transistor of a target pixel to a voltage level representing a logical on state, wherein the select transistor is the only transistor in the target pixel that is directly connected to the column conductor; and

for each sub pixel in the target pixel:

driving the voltage on row conductors connected to switching transistors, if any, that are located between the column conductor and the sub pixel to a voltage level that represents the logical on state;

driving the voltage on a column conductor connected to the target pixel to a voltage level representing a logical light state or dark state for the sub pixel; and

after the sub pixel has been charged to a voltage corresponding to the voltage on the column conductor, driving the voltage on the row conductor connected to the switching transistor associated with the sub pixel to a voltage level representing the logical off state.

34. (new) The method of claim 33, wherein the switching transistors of the target pixel are arranged in series, and wherein driving the display device in the second mode comprises initially driving the voltage on all row conductors connected to the target pixel to the logical on state and then driving the voltages on the row conductors to the logical off state one

row conductor at a time as the sub pixels are charged in order from farthest from the column conductor to closest to the column conductor.

35. (new) The method of claim 33, wherein the select transistor is the switching transistor associated with one of the sub pixels and that sub pixel is charged last.